## REMARKS

This paper responds to the Office Action mailed on July 29, 2005.

None of the claims are amended. Claim 35 is canceled without disclaimer or prejudice. As a result, claims 10-22, and 31-34 are now pending in this application.

### *§112 Rejection of the Claims*

Claim 35 was rejected under 35 USC § 112, second paragraph, as being indefinite for omitting essential step. Applicant respectfully traverses. However, to expedite prosecution, Applicant cancels claim 35 without disclaimer or prejudice.

### *§102 Rejection of the Claims*

**Claims 31 and 33 were rejected under 35 USC § 102(b) as being anticipated by Wood et al. (U.S. 4,246,656).**

Applicant respectfully traverses for the reasons presented in previous amendment and responses and for additional reasons below.

Claim 31 recites, among other things, performing a logic function on a plurality of bits "held by the register circuits" to produce a "rotation number", and aligning a plurality of output bits provided at one of the output nodes with a plurality of output bits provided at other output nodes, "based on the rotation number", when the plurality of input bits received at the input nodes are misaligned by at least one bit time interval.

Wood teaches a correlation counter 66 (FIG. 1 and FIG. 3) to control counts of counters 58 and 60 (FIG. 1). In response to counters 58 and 60, 8-bit multiplexers 54 and 56 (FIG. 1) select input lines connected to corresponding 8-bit shift registers 50 and 52 to select data in 8-bit shift registers 50 and 52. Applicant is unable to find in Wood that correlation counter 66 and/or counters 58 and 60 provide a "rotation number" to align a plurality of output bits provided at one of the output nodes with a plurality of output bits provided at other output nodes, "based on the rotation number", when the plurality of input bits received at the input nodes are misaligned by at least one bit time interval. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 31.

Dependent claim 33 depends on independent claim 31. As presented above, claim 31 is patentable over Wood. Thus, claim 33 is also patentable over Wood for at least the reasons presented above regarding claim 31, plus the things recited in claim 33 such as "wherein each of the register circuits further includes a select circuit connected to a subset of the number of register cells through a number of select lines". Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 33.

*§103 Rejection of the Claims*

**Claim 10 was rejected under 35 USC § 103(a) as being unpatentable over Taya et al. (U.S. 5,778,214) in view of Yamamoto et al. (JP 06-120937).**

Applicant respectfully traverses for the reasons presented in previous amendment and responses and for additional reasons below.

Claim 10 recites, among other things, a plurality of register circuits and "each of the register circuits being connected between one of the input nodes and one of the output nodes to receive a plurality of input bits at one of the input nodes and to provide at one of the output nodes a plurality of output bits based on the plurality of input bits".

Taya teaches, in FIG. 2, a plurality of shift registers 22a, 22b, and 22c. FIG. 2 of Taya shows that *all* of the input nodes of shift registers 22a, 22b, and 22c receive data from the same node (node common to output node of SW 12a, SW 12b, SW 12c, and SW 12n). Page 19 of the Office Action states that the Examiner disagrees and submits that FIG. 2 of Taya also shows output nodes SW 12b-n (besides output node SW 12a, as previously indicated by Applicant). However, as previously indicated, Applicant respectfully submits that output nodes of SW 12a, SW 12b, SW 12c, and SW 12n of Taya are the same node to which shift registers 22a, 22b, and 22c of Taya are connected. Applicant is unable to find in Taya and Yamamoto, either individual or in combination, "each of the register circuits being connected between one of the input nodes and one of the output nodes to receive a plurality of input bits at one of the input nodes and to provide at one of the output nodes a plurality of output bits based on the plurality of input bits". Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 10.

**Claim 11 was rejected under 35 USC § 103(a) as being unpatentable over Taya et al. (U.S. 5,778,214) and Yamamoto et al. (JP 06-120937) as applied to claim 10 above, and further in view of Fukuoka (U.S. 6,467,063).**

Applicant respectfully traverses for the reasons presented in previous amendment and responses and for additional reasons below.

Dependent claim 11 depends on independent claim 10. As presented above, claim 10 is patentable over Taya and Yamamoto, either individual or in combination. Thus, claim 11 also is also patentable over Taya and Yamamoto, either individual or in combination, for at least the reasons presented above regarding claim 10. Claim 11 is also patentable over Taya, Yamamoto, and Fukuoka, either individual or in combination, for at least the reasons presented above regarding claim 10, plus the things recited in claim 11 such as "each of the register circuits includes a number of register cells, wherein the number of register cells equals 2M-1, where M is a maximum number of bit time intervals of misalignment of a parallel bus that connects to the integrated circuit". Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 11.

**Claims 12-13 were rejected under 35 USC § 103(a) as being unpatentable over Fukuoka, Taya, and Yamamoto as applied to claim 11 above, and further in view of Moriwaki et al. (U.S. 6,753,872).**

Applicant respectfully traverses for the reasons presented in previous amendment and responses and for additional reasons below.

Dependent claim 12 depends on dependent claim 11. As presented above, claim 11 is patentable over Taya, Yamamoto, and Fukuoka, either individual or in combination. Thus, claim 12 also is also patentable over Taya, Yamamoto, and Fukuoka, either individual or in combination, for at least the reasons presented above regarding claim 11. Claim 12 is also patentable over Taya, Yamamoto, and Fukuoka in view of Moriwaki, either individual or in combination, for at least the reasons presented above regarding claim 11, plus the things recited in claim 12 such as "each of the register circuits further includes a select circuit connected to a subset of the number of register cells through a number of select lines". Notwithstanding, the above reasons, Applicant further notes that in FIG. 5 of Moriwaki, each of the registers, such as register 50-1, has 24 bits (Moriwaki, column 9, line 11); and selector 51 of Moriwaki connects to

all 24 bits of each register through a 24-bit bus 24b. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 12.

Dependent claim 13 depends on dependent claim 12. As presented above, claim 12 is patentable over Taya, Yamamoto, and Fukuoka in view of Moriwaki, either individual or in combination. Thus, claim 13 also is also patentable over Taya, Yamamoto, and Fukuoka in view of Moriwaki, either individual or in combination, for at least the reasons presented above regarding claim 12, plus the things recited in claim 13 such as "the number of select lines equals a maximum number of bit time intervals of misalignment of a parallel bus that connects to the integrated circuit". Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 13.

**Claims 14 and 16-17 were rejected under 35 USC § 103(a) as being unpatentable over Wood, in view of Yamamoto and Fukuoka.**

Applicant respectfully traverses for the reasons presented in previous amendment and responses and for additional reasons below.

Claims 14 recites, among other things, a select circuit, and logic circuit, wherein the logic circuit includes a calculation unit to perform the logic function on a plurality of bits, a plurality of memory units to store results from the logic function, a counter to count values stored in the memory units, and a detect logic to determine results from the counter and to generate a rotation number, the rotation number being used to rotate data held in the number of register cells.

The Office Action asserts that Wood teaches the above elements. Applicant is unable to find in Wood each and every element of claim 14, as recited above.

The Office Action compares a counter (counter 58 or 60 in FIG. 1) of Wood to the counter of claim 14. However, the Office Action also uses the same counter of Wood to compare to the plurality of memory units recited in claim 14.

The Office Action compares an 8-bit multiplexer (multiplexer 54 or 56 of FIG. 1) of Wood to the select circuit of claim 14. However, the Office Action also uses the same counter and the same 8-bit multiplexer of Wood to compare to the detection logic of claim 14.

Since the Office Action uses the same single element in Wood to compare to multiple elements of claim 14, at least one element of claim 14 is missing from Wood. Thus, Wood does not teach each and every element of claim 14.

Claim 14 also recites a plurality of register circuits in which each of the register circuits includes a number of register cells and the select circuit being connected to a "subset of the number of register cells" through a number of select lines.

Wood shows in FIG. 1 an 8-bit multiplexer 54 connected to an 8-bit shift register 50 through eight input lines, and an 8-bit multiplexer 56 connected to an 8-bit shift register 52 through eight input lines. In column 5, lines 6-12, Woods describes,

"eight-bit shifter registers are hold[ing] eight bits of data. The eight stages of each shift register are connected to corresponding inputs on associated eight-bit multiplexers 54 and 56. In connection with multiplexer 54, a binary counter 58 is used to address a particular data stage connected to one of the eight input lines from the eight-bit shift register 50."

Thus, in Wood, the 8-bit multiplexer (e.g., 8-bit multiplexer 54) connects to *all eight bits* of the corresponding 8-bit shift register (e.g., 8-bit shift register 50) through the eight inputs lines. In contrast, claim 14 recites that the select circuit is connected to a "subset of the number of register cells" through a number of select lines.

Applicant is also unable to find in Wood, Yamamoto, and Fukuoka, either individual or in combination, a select circuit connected to a "subset of the number of register cells" through a number of select lines, as claimed in claim 14.

Notwithstanding the reasons presented above, Applicant submits that claim 61 is patentable over Wood, Yamamoto, and Fukuoka, for the reasons presented as follows.

Claim 14 further recites a detect logic to determine results from the counter and to generate a rotation number, "the rotation number being used to rotate data held in the number of register cells".

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The *Fine* court stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413,

> 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

The M.P.E.P. adopts this line of reasoning, stating that

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

An invention can be obvious even though the suggestion to combine prior art teachings is not found in a specific reference. *In re Oetiker*, 24 USPQ2d 1443 (Fed. Cir. 1992). At the same time, however, although it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979)).

Applicant respectfully submits that there is no motivation to alter Wood in view of Yamamoto and Fukuoka. A factor cutting against a finding of motivation to combine or modify the prior art is when the prior art teaches away from the claimed combination. A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the office action, or would be led in a direction divergent from the path the applicant took. *In re Gurley*, 27 F.3d 551, 31 USPQ 2d 1130, 1131 (Fed. Cir. 1994); *United States v. Adams*, 383 U.S. 39, 52, 148 USPQ 479, 484 (1966); *In re*

*Sponnoble*, 405 F.2d 578, 587, 160 USPQ 237, 244 (C.C.P.A. 1969); *In re Caldwell*, 319 F.2d 254, 256, 138 USPQ 243, 245 (C.C.P.A. 1963).

Wood uses an 8-bit shift register (e.g., 8-bit shift register 52) to hold eight bits of data. Wood uses and an 8-bit multiplexer (e.g., 8-bit multiplexer 56) to select data from the 8-bit shift register by advancing the input tap position of the 8-bit multiplexer to select new data output lines from the 8-bit shift register. See Wood, column 5, lines 28-32. Thus, the eight bits of data in the 8-bit shift register of Wood are *fixed* so that each of the eight bits of data may be selected to set an appropriate delay in Wood's system. One of ordinary skill in the art at the time of the present invention would not be motivated to go against the teachings of Wood. That is, one of skill in the art would have no motivation to alter Wood to *shift* the eight bits of data held in the 8-bit shift register of Wood.

Based on the reasons presented above, Applicant submits that claim 14 is patentable over Wood in view of Yamamoto and Fukuoka. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 14.

Dependent claim 16 depends on independent claim 14. As presented above, claim 14 is patentable over Wood in view of Yamamoto and Fukuoka. Thus, claim 16 is also patentable over Wood in view of Yamamoto and Fukuoka for at least the reasons presented above regarding claim 14, plus the things recited in claim 16 such as "the memory units are arranged in rows and columns, wherein the memory units in the same row form a shift register". Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 16.

The Office Action states that the Examiner takes Official Notice that it is well known in the art to arrange memory units in rows and columns, wherein the memory units in the same row form a shift register. Applicant respectfully traverses the taking of Official Notice and, pursuant to M.P.E.P. § 2144.03, Applicant requests documents or an affidavit to support the rejection of claim 16. In the absence of documents or an affidavit to support the rejection of claim 16, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 16.

Dependent claim 17 depends on independent claim 14. As presented above, claim 14 is patentable over Wood in view of Yamamoto and Fukuoka. Thus, claim 17 is also patentable over Wood in view of Yamamoto and Fukuoka for at least the reasons presented above regarding

claim 14, plus the things recited in claim 17. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 17.

**Claim 15 was rejected under 35 USC § 103(a) as being unpatentable over Taya et al. (U.S. 5,778,214) and Yamamoto et al. (JP 06-120937) as applied to claim 10 above, and further in view of Jaquette (U.S. 5,737,371).**

Applicant respectfully traverses for the reasons presented in previous amendment and responses and for additional reasons below.

Dependent claim 15 depends on independent claim 10. As presented above, claim 10 is patentable over Taya and Yamamoto, either individual or in combination. Thus, claim 15 also is also patentable over Taya and Yamamoto, either individual or in combination, for at least the reasons presented above regarding claim 10. Claim 15 is also patentable over Taya, Yamamoto, and Jaquette, either individual or in combination, for at least the reasons presented above regarding claim 10, plus the things recited in claim 15. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 15.

**Claims 18-20 were rejected under 35 USC § 103(a) as being unpatentable over Moriwaki in view of Grondalski (U.S. 6,108,763) and Wood.**

Applicant respectfully traverses for the reasons presented in previous amendment and responses and for additional reasons below.

Claim 18, recites among other things, a shift register including a plurality of register cells, and a select circuit connected to "a subset of the number of register cells" through a number of select lines.

Moriwaki teaches, in FIG. 5, a selector 51 connected to each of the register circuits 50-1 through 50-64 through select lines 24b (24 bits). Column 9, lines 11 of Moriwaki states that each of the register circuits 50-1 through 50-64 has a capacity of 24 bits. Thus, selector 51 of Moriwaki is connected to *all* bits of each of the register circuits 50-1 through 50-64. As discussed in claim 14, in Wood teaches an 8-bit multiplexer (e.g., 8-bit multiplexer 54) which connects to *all eight bits* of a corresponding 8-bit shift register (e.g., 8-bit shift register 50) through the eight inputs lines.

Based on at least the reasons above, Applicant is unable to find in Moriwaki, Grondalski, and Wood, either individual or in combination, a select circuit connected to "a subset of the

number of register cells" through a number of select lines, as claimed in claim 18. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 18.

Dependent claim 19 depends on independent claim 18. As presented above, claim 18 is patentable over Moriwaki, Grondalski, and Wood, either individual or in combination. Thus, claim 19 also is also patentable over Moriwaki, Grondalski, and Wood, either individual or in combination, for at least the reasons presented above regarding claim 18, plus the things recited in claim 19. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 19.

Dependent claim 20 depends on claim 19. As presented above, claim 19 is patentable over Moriwaki, Grondalski, and Wood, either individual or in combination. Thus, claim 20 also is also patentable over Moriwaki, Grondalski, and Wood, either individual or in combination, for at least the reasons presented above regarding claim 19, plus the things recited in claim 20. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 20.

**Claim 21 was rejected under 35 USC § 103(a) as being unpatentable over Wood, Moriwaki, and Grondalski as applied to claim 19 above, and further in view of Barnsley et al. (U.S. 5,730,812).**

Dependent claim 21 depends on claim 19. As presented above, claim 19 is patentable over Moriwaki, Grondalski, and Wood, either individual or in combination. Thus, claim 21 also is also patentable over Moriwaki, Grondalski, and Wood, either individual or in combination, for at least the reasons presented above regarding claim 19. Claim 21 also is also patentable over Moriwaki, Grondalski, Wood, and Barnsley, either individual or in combination, for at least the reasons presented above regarding claim 19, plus the things recited in claim 21. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 21.

**Claim 22 was rejected under 35 USC § 103(a) as being unpatentable over Wood, Moriwaki, and Grondalski as applied to claim 19 above, and further in view of Frisch et al. (U.S. 4,707,834).**

Dependent claim 22 depends on claim 19. As presented above, claim 19 is patentable over Moriwaki, Grondalski, and Wood, either individual or in combination. Thus, claim 22 also is also patentable over Moriwaki, Grondalski, and Wood, either individual or in combination, for

at least the reasons presented above regarding claim 19. Claim 22 also is also patentable over Moriwaki, Grondalski, Wood, and Frisch, either individual or in combination, for at least the reasons presented above regarding claim 19, plus the things recited in claim 22. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 22.

**Claims 32 and 34 were rejected under 35 USC § 103(a) as being unpatentable over Wood as applied to claim 31 above, and further in view of Fukuoka.**

Dependent claim 32 depends on independent claim 31. As presented above, claim 31 is patentable over Wood. Thus, claim 32 is also patentable over Wood for at least the reasons presented above regarding claim 31. Claim 32 is also patentable over Wood in view of Fukuoka for at least the reasons presented above regarding claim 31, plus the things recited in claim 32 such as "each of the register circuits includes a number of register cells, wherein the number of register cells equals 2M-1, where M is a maximum number of bit time intervals of misalignment of a parallel bus that connects to the register circuits". Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 32.

Dependent claim 34 depends on claim 33. As presented above, claim 33 is patentable over Wood. Thus, claim 34 is also patentable over Wood for at least the reasons presented above regarding claim 33. Claim 34 is also patentable over Wood in view of Fukuoka for at least the reasons presented above regarding claim 33, plus the things recited in claim 34 such as "wherein the number of select lines equals a maximum number of bit time intervals of misalignment of a parallel bus that connects to the register circuits". Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 34.

**Claim 35 was rejected under 35 USC § 103(a) as being unpatentable over Wood as applied to claim 31 above, and further in view of Yamamoto.**

Applicant does not admit that Wood and Yamamoto, either individual or in combination, are prior art with respect to claim 35. However, as indicated above, Applicant cancels claim 35 without disclaimer or prejudice.

*Conclusion*

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

MATTHEW B. HAYCOCK ET AL.

By their Representatives,
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 349-9592

Date 29 November 2005 By _____
Viet V. Tong
Reg. No. 45,416

I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

_____ November 29, 2005
Amy J. Moriarty Date of Transmission